RP2350

RP2350A
RP2350B
RP2354A
RP2354B

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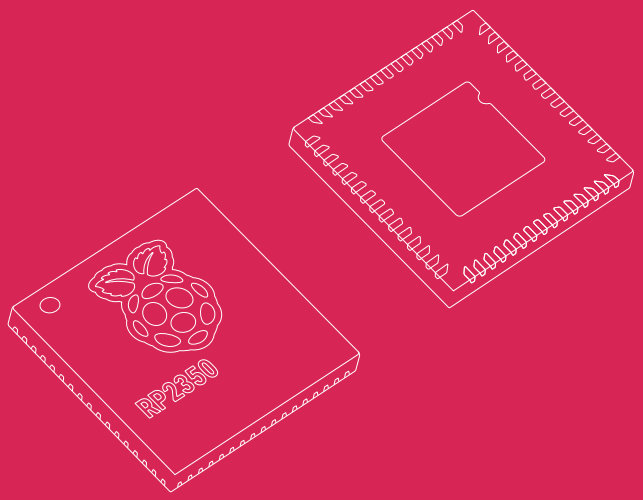
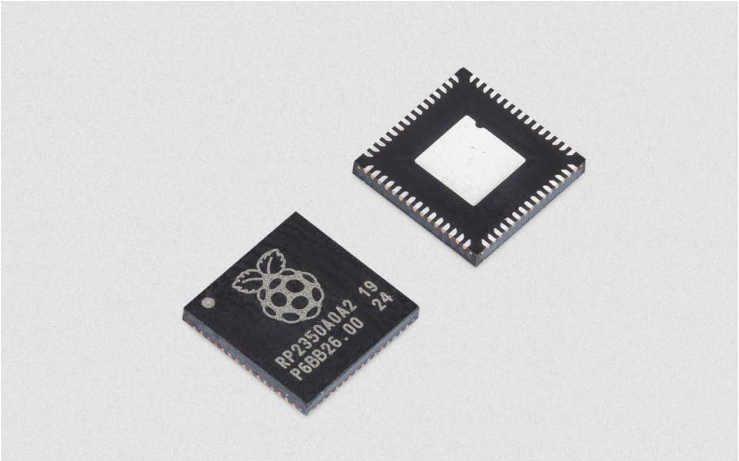


Raspberry Pi Ltd

Overview



RP2350 is the new high-performance, secure microcontroller from Raspberry Pi. With a higher core clock speed, double the on-chip SRAM, more powerful Arm cores, optional RISC-V cores, new security features, and upgraded interfacing capabilities, RP2350 delivers a significant performance and feature boost over its predecessor, RP2040.

RP2350 provides a comprehensive security architecture, built around Arm TrustZone for Cortex-M, and incorporating signed boot, 8KB of antifuse OTP for key storage, SHA-256 acceleration, a hardware TRNG, and fast glitch detectors. These features, including the secure boot ROM, are extensively documented and available to all users without restriction: this transparent approach, which contrasts with the “security through obscurity” offered by legacy vendors, allows professional users to integrate RP2350 into products with confidence.

The unique dual-core, dual-architecture capability of RP2350 allows users to choose between a pair of industry-standard Arm Cortex-M33 cores, and a pair of open-hardware Hazard3 RISC-V cores. Three high-performance Programmable I/O (PIO) co-processors, with a total of twelve independent state machines, support software-defined interfacing, with little or no CPU overhead.

RP2350 offers best-in-class performance for a vast range of applications, from cost-optimised embedded computing, to secure applications requiring trusted firmware, to industrial IoT deployments with demanding I/O requirements. It is available in four package variants: with 30 or 48 GPIO pins, and with or without 2MB stacked flash memory.

Key features

CPU:

Dual Arm Cortex-M33 or dual Hazard3 RISC-V processors @ 150MHz

Memory:

- 520 KB on-chip SRAM, in ten independent banks
- Support for up to 16 MB of external QSPI flash/PSRAM via dedicated QSPI bus; additional 16 MB flash/PSRAM accessible via optional second chip-select

Peripherals:

- 2 × UART
- 2 × SPI controllers
- 2 × I2C controllers
- 24 × PWM channels
- 4/8 × ADC channels
- 1 × USB 1.1 controller and PHY, with host and device support
- 12 × PIO state machines

Security features:

- Optional boot signing, enforced by on-chip mask ROM, with key fingerprint in OTP
- Protected OTP storage for optional boot decryption key
- Global bus filtering based on Arm or RISC-V security/privilege levels
- Peripherals, GPIOs, and DMA channels individually assignable to security domains
- Hardware mitigations for fault injection attacks
- Hardware SHA-256 accelerator

Package:

Product	Package	Internal flash	GPIO	Analogue inputs
RP2350A	QFN-60	None	30	4
RP2350B	QFN-80	None	48	8
RP2354A	QFN-60	2 MB	30	4
RP2354B	QFN-80	2 MB	48	8

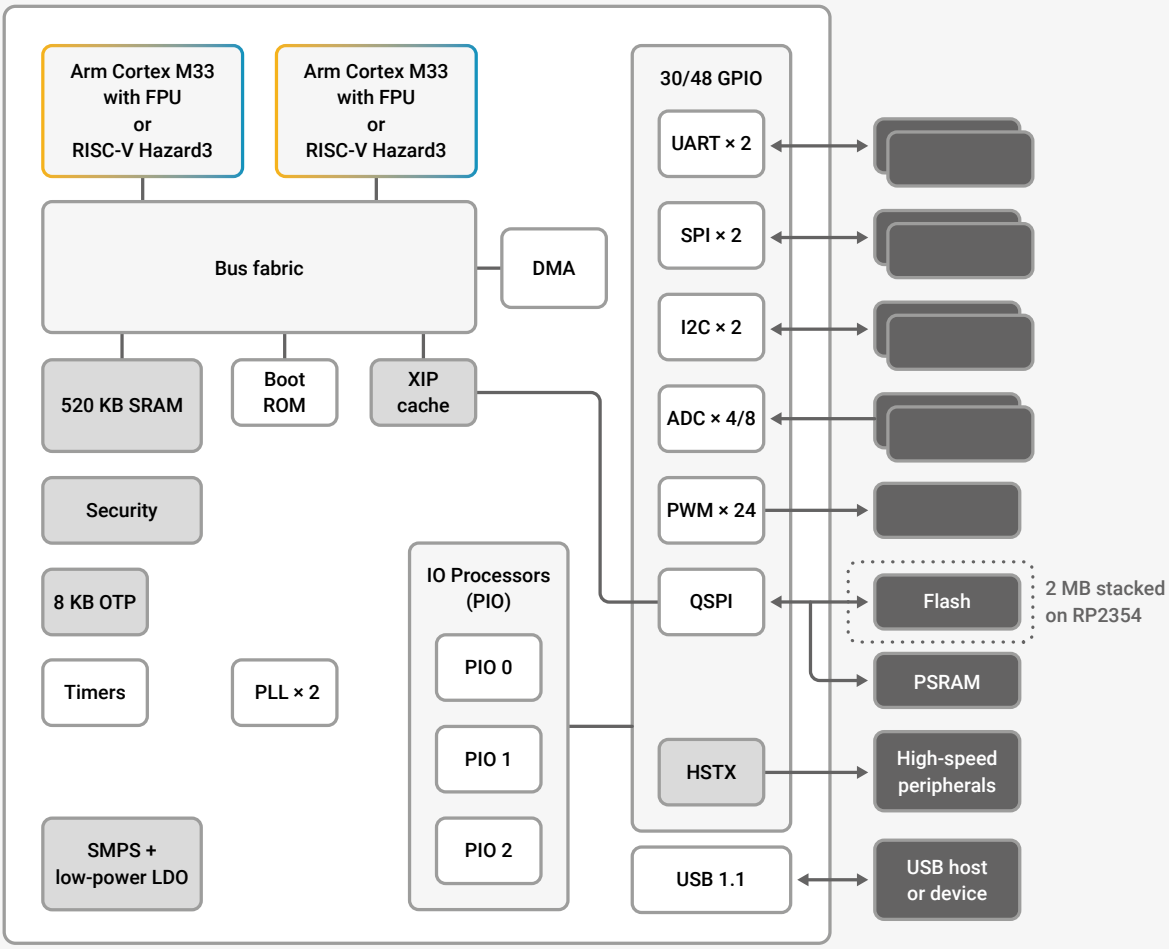
Production lifetime:

Raspberry Pi understands the value to customers of long-term product availability and therefore aims to continue supply for as long as practically possible. We expect RP2350 to remain in production until at least January 2045.

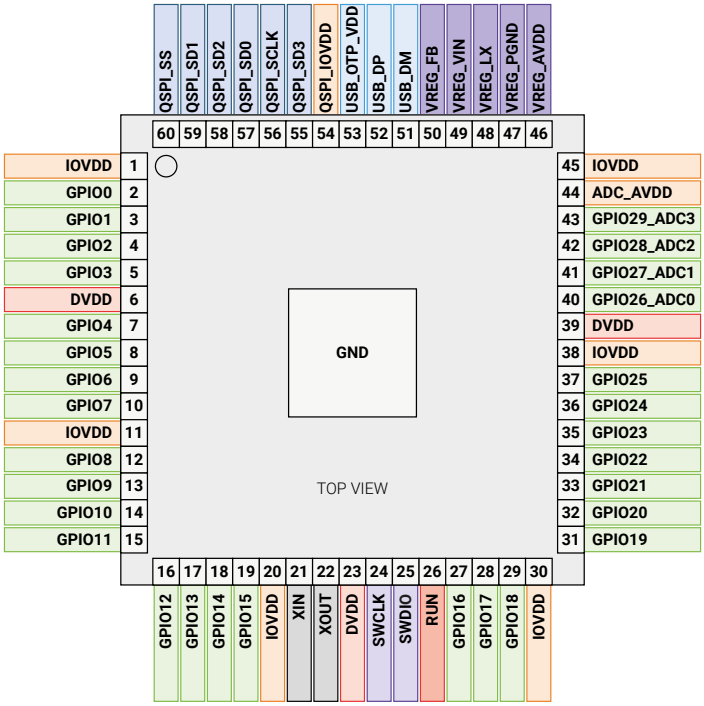
Compliance:

For a full list of local and regional product approvals, please visit pip.raspberrypi.com

RP2350 block diagram



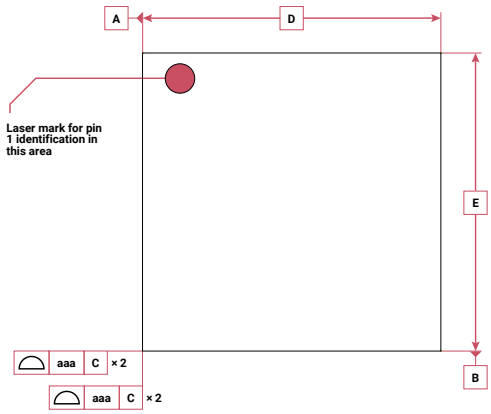
60QFN pinout



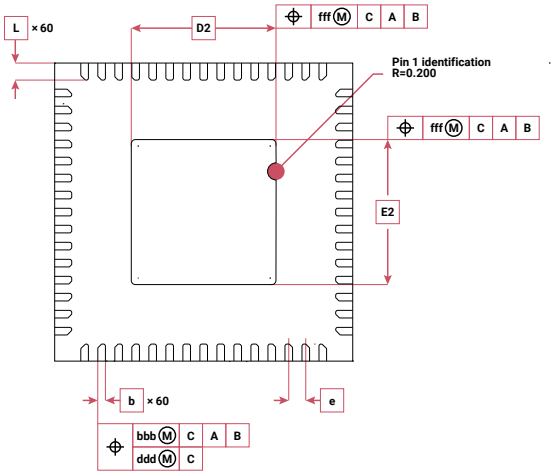
GPIOx	General-purpose digital input and output
GPIOx/ADCy	General-purpose digital input and output, with analogue-to-digital converter function
QSPIx	Interface to an SPI, Dual-SPI or Quad-SPI flash device, with execute-in-place support
USB_DM and USB_DP	USB controller, supporting full-speed device and full-/low-speed host
XIN and XOUT	Connect a crystal to RP2350's crystal oscillator
RUN	Global asynchronous reset pin; reset when driven low, run when driven high
SWCLK and SWDIO	Access to the internal Serial Wire Debug multi-drop bus; provides debug access to both processors
GND	Single external ground connection, bonded to a number of internal ground pads on the RP2350 die
QSPI_IOVDD	Provides the IO supply for the chip's QSPI interface
IOVDD	Power supply for digital GPIOs, nominal voltage 1.8 V to 3.3 V
USB_OTP_VDD	Power supply for internal USB full-speed PHY and OTP, nominal voltage 3.3 V
ADC_AVDD	Power supply for analogue-to-digital converter, nominal voltage 3.3 V
VREG_VIN	Power input for the internal core voltage regulator, nominal voltage 2.7 V to 5.5 V
VREG_FB	Internal core voltage regulator: See datasheet
VREG_LX	Internal core voltage regulator: See datasheet
VREG_PGND	Internal core voltage regulator: See datasheet
VREG_AVDD	Internal core voltage regulator: See datasheet
DVDD	Digital core power supply, nominal voltage 1.1 V

60QFN physical specification

Top view



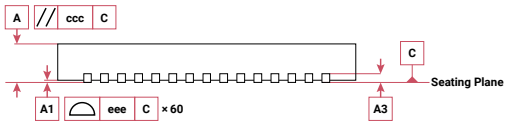
Bottom view



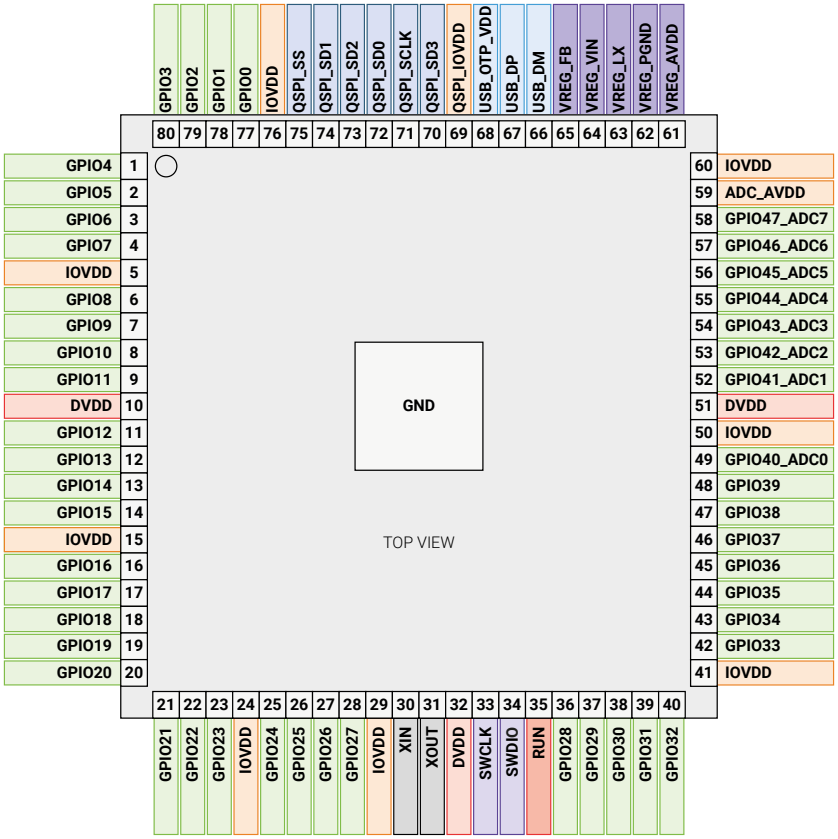
Symbol	Millimetre		
	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	-	0.050
A3	0.203 REF		
D	7 BSC		
E	7 BSC		
D2	3.350	3.400	3.450
E2	3.350	3.400	3.450
b	0.130	0.180	0.230
e	0.400 BSC		
L	0.350	0.400	0.450
Tolerances of form and position			
aaa	0.050		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

All dimensions are in millimetres
Drawings not to scale

Side view



80QFN pinout



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80QFN physical specification

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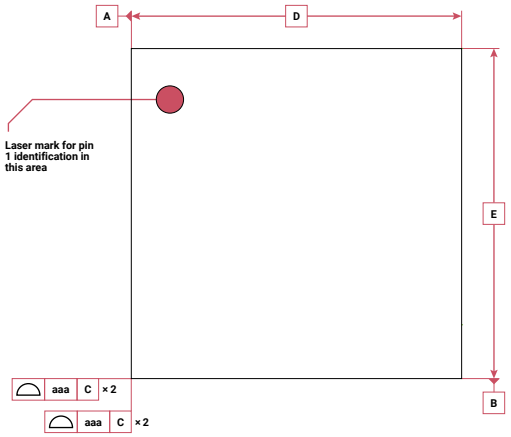
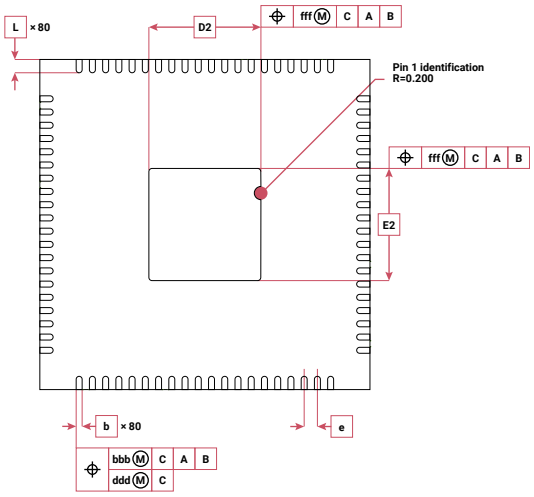


Bottom view



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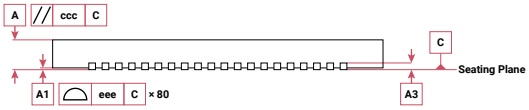
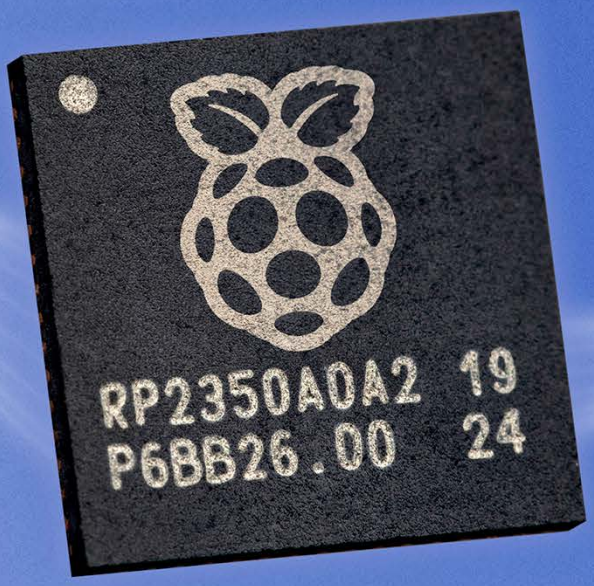


SAFETY INSTRUCTIONS

To avoid malfunction or damage to this product, please observe the following:

- Anti-static precautions shall be taken when handling.
- Do not expose to water or moisture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